ISO9001:2000 Certified SCI Quality System

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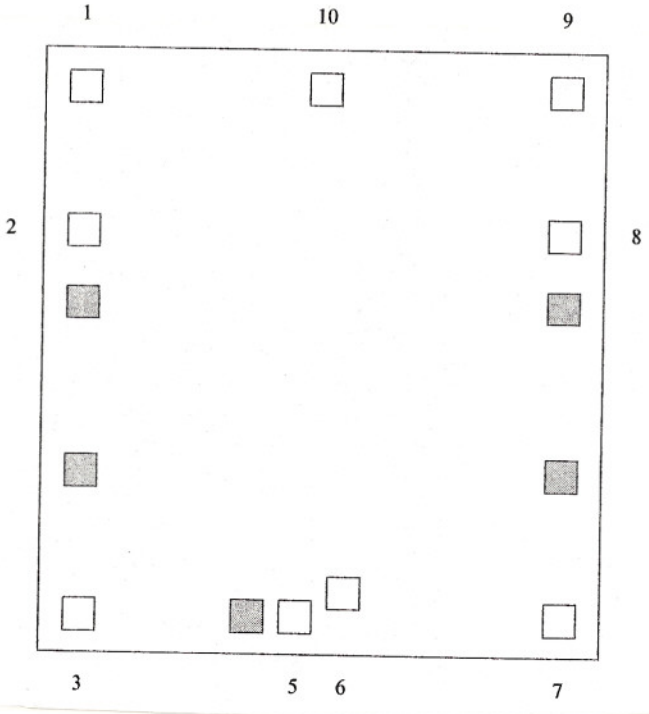
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD	FUNCTION
1	D1
2	S1
3	IN1
4	NC
5	GND
6	V –
7	IN2
8	S2
9	D2
10	V +

NC = NO CONNECT

NOTE:
Chip back must be connected to V+

Topside Metal: Al
Backside: Si
Backside Potential: See Above
Mask Ref: -
Bond Pads : .004" min.

APPROVED BY: CD	**DIE SIZE : .088" x .098"**	**DATE: 6/28/02**
MFG: Intersil	**THICKNESS: .020" ± .003"**	**P/N: DG300A**